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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/530,888	04/11/2005	Yasuyuki Suzuki	F2371.0045	3240

32172 7590 12/21/2005

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EXAMINER	
CRAWFORD, JASON	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/530,888	SUZUKI, YASUYUKI	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *1-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16,17,19-25,27,29,30,32-38 and 40* is/are rejected.

7)☒ Claim(s) *18,26,28,31,39 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Miscellaneous

Claims 1-15 were cancelled by request of the applicant, therefore only the new amended Claims 17-36 are to be examined below for this application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 17, 19, 24, 25, 27, 29, 30, 32, 37, 38 and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada (US 6046653).

In regards to Claim 16, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance of 30Ω (Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance

of signal transmission line (13) (Column 9 Lines 66-67) is higher than the first impedance of 30Ω.

In regards to Claim 17, Yamada discloses of the IC elements (3A, 3B) including a plurality of IC element groups (inherent in Fig 5 as bidirectional buffers 10', 20').

In regards to Claim 19, Yamada discloses of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

In regards to Claim 24, Yamada discloses of the IC elements (3A, 3B) of being of semiconductor (LSI) type (Column 6 Lines 32-35 and Column 9 Lines 23, 29) wherein it would be obvious to one of ordinary skill in the art that these semiconductor devices would be of bare chip type, i.e. they are silicon manufactured IC chips.

In regards to Claim 25, Yamada discloses of IC elements (3A, 3B) being semiconductor devices (LSI, Column 1 Lines 21-25 and Column 9 Lines 23, 29) where these devices would be considered by anyone of ordinary skill in the art to be bare chip devices, i.e. a manufactured IC silicon chips that can be configured to a printed circuit board (1).

In regards to Claim 27, Yamada discloses of the matching characteristic impedance of 50Ω, which is not more ten times larger than the first impedance of 30Ω (Column 9 Lines 62-67 and Column 10 Lines 1-3).

In regards to Claim 29, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal

transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance and second impedance each of which are 30Ω (Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance of signal transmission line (13) (Column 9 Lines 66-67) is higher than both of the lower first and second impedances of 30Ω.

In regards to Claim 30, Yamada discloses of the IC elements (3A, 3B) including a plurality of IC element groups (inherent in Fig 5 as bidirectional buffers 10', 20').

In regards to Claim 32, Yamada discloses of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

In regards to Claim 37, Yamada discloses of the IC elements (3A, 3B) of being of semiconductor (LSI) type (Column 6 Lines 32-35 and Column 9 Lines 23, 29) wherein it would be obvious to one of ordinary skill in the art that these semiconductor devices would be of bare chip type, i.e. they are silicon manufactured IC chips.

In regards to Claim 38, Yamada discloses of IC elements (3A, 3B) being semiconductor devices (LSI, Column 1 Lines 21-25 and Column 9 Lines 23, 29) where these devices would be considered by anyone of ordinary skill in the art to be bare chip devices, i.e. a manufactured IC silicon chips that can be configured to a printed circuit board (1).

In regards to Claim 40, Yamada discloses of the matching characteristic impedance of 50Ω, which is not more ten times larger than the first impedance of 30Ω (Column 9 Lines 62-67 and Column 10 Lines 1-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20, 21, 23, 33, 34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 6046653) in view of Suzuki (US 6781404).

In regards to Claims 20, 21 and 23, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance of 30Ω (Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance of signal transmission line (13) (Column 9 Lines 66-67) is

higher than the first impedance of 30Ω. Yamada also disclose of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

. Yamada does not directly disclose of an the semiconductor device being an ECL circuit with the output circuit being a differential circuit and the input circuit being an emitter-follower circuit with a resistance element connected between the base and a ground or the base and a power source.

Suzuki discloses of an ECL semiconductor device (Column 1 Lines 37-41, Fig 1) comprised of an output circuit being a differential switching circuit (Column 1 Lines 40-42, Column 9 Lines 64-67) having an input circuit that is an emitter-follower circuit (Column 9 Lines 52-54) having a resistance element (114) connected between a base and a power source (117) (Fig 1, 8).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have an ECL circuit with the output circuit being a differential circuit and the input circuit being an emitter-follower as taught by Suzuki to utilize the high speed operations of an ECL circuit by reducing interconnect delay time.

In regards to Claims 33, 34 and 36, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance and second impedance each of which are 30Ω

(Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance of signal transmission line (13) (Column 9 Lines 66-67) is higher than both of the lower first and second impedances of 30Ω.). Yamada also disclose of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

Yamada does not directly disclose of an the semiconductor device being an ECL circuit with the output circuit being a differential circuit and the input circuit being an emitter-follower circuit with a resistance element connected between the base and a ground or the base and a power source.

Suzuki discloses of an ECL semiconductor device (Column 1 Lines 37-41, Fig 1) comprised of an output circuit being a differential switching circuit (Column 1 Lines 40-42, Column 9 Lines 64-67) having an input circuit that is an emitter-follower circuit (Column 9 Lines 52-54) having a resistance element (114) connected between a base and a power source (117) (Fig 1, 8).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have an ECL circuit with the output circuit being a differential circuit and the input circuit being an emitter-follower as taught by Suzuki to utilize the high speed operations of an ECL circuit by reducing interconnect delay time.

Claims 22 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada (US 6046653) in view of Mizukami (US 5111080).

In regards to Claim 22, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance of 30Ω (Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance of signal transmission line (13) (Column 9 Lines 66-67) is higher than the first impedance of 30Ω. Yamada also disclose of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

Yamada does not directly disclose of the input circuit being an source-follower circuit with a resistance element connected between the base and a ground or the base and a power source.

Mizukami discloses of an impedance matching circuit with a signal receiving input stage (UBR, Fig 1) having a source-follower circuit (LS) comprised of transistors (Q5, Q6) (Column 8 Lines 6-8).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the input circuit being a source-follower as taught by Mizukami to ensure that the signals are no longer level-biased by a power source so that they can perform adequate amplifying operations.

In regards to Claim 35, Yamada discloses of a semiconductor device comprising of an input stage IC element (3A, comprised of bidirectional input/output buffer 10' in Fig 5) and an output stage IC element (3B, comprised of bidirectional input/output buffer 20' in Fig 5) mounted onto a common mounting substrate/board (1, Fig 6) with signal transmission paths (13, 16 and 19) that connect the two elements to achieve impedance matching. Yamada also discloses of the input/output impedances of (3A, 3B) equaling a first impedance of 30Ω (Column 9 Lines 62-64), which is impedance matched to one of the signal transmissions paths (13) by the use of (16, 19 which are 10Ω/cm*2cm, Column 10 Line 4). Therefore the matching impedance is 50Ω to match the impedance of signal transmission line (13) (Column 9 Lines 66-67) is higher than the first impedance of 30Ω. Yamada also disclose of at least one of the IC elements having a resistance element (120 or 121) for impedance matching (Fig 7).

Yamada does not directly disclose of the input circuit being an source-follower circuit with a resistance element connected between the base and a ground or the base and a power source.

Mizukami discloses of an impedance matching circuit with a signal receiving input stage (UBR, Fig 1) having a source-follower circuit (LS) comprised of transistors (Q5, Q6) (Column 8 Lines 6-8).

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to have the input circuit being a source-follower as taught by Mizukami to ensure that the signals are no longer level-biased by a power source so that they can perform adequate amplifying operations.

Allowable Subject Matter

Claims 18, 26, 28, 31, 39 and 41 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to Claims 18 and 31, the prior art does not directly disclose of the matching impedance differing between two of the signal transmission paths, nor would it have been obvious to one of ordinary skill in the art to do so.

In regards to Claims 26 and 39, the prior art does not directly disclose of the semiconductor device in accordance to Claim 16 wherein the input signal has a transmission rate not less than 1 Gbps and a frequency not less than 800 Mhz, nor would it have been obvious to one of ordinary skill in the art to do so.

In regards to Claims 28 and 41, the prior art does not directly disclose of the matching impedance not being less than double of the said first impedances, nor would it have been obvious to one of ordinary skill in the art to do so.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SPE Rex Barnie

JMC